steps (c-5) and (c-8) are performed in parallel with the operation at step (c-4); however, error correction for the data on the buffer memory 4 is not performed because an error-containing code has not been detected.

The error detecting process done by the error detector 7 is complete at step (c-4), and the error detection signal 111 is transmitted to the system control unit 1 so as to inform whether an error has been detected or not. In this case, steps (c-9) through (c-12) are not executed.

Through these steps, the horizontal error correction for one sector is complete. In the same manner, horizontal error correction for the subsequent 15 sectors is executed so as to complete the horizontal error correction for one block. If no error is detected from all sectors, the error correcting operation is complete; if there is an error detected even from one sector, the next process including vertical error correction will be executed.

As described hereinbefore, in the present embodiment, data are transferred from the buffer memory 4 not only to the syndrome calculator 5 but also to the error detector 7 at the same time, and the error detector 7 executes error detection concurrently with syndrome calculation. If an error-containing code is not detected in one sector in the syndrome calculation, the subsequent operations become unnecessary, which greatly reduces the time required for error correction. Hence, the present invention will become more significant when probable technological development in the future reduces the error rate.

Unlike Embodiment 1, the mid-term result register 8, which is more expensive than memory, becomes unnecessary.

(Embodiment 3)

The present embodiment differs from the prior art in that the syndrome calculator 5 outputs the error-containing code detection signal 22, which indicates that an error-containing code word has been detected, to the DMA control unit 2 and to the error detector 7; the error corrector 6 outputs the error-containing code word signal 23 to the DMA control unit 2 and to the error detector 7; and that the mid-term result register 8 is provided.

Figure 9 shows the structure of the error correction device of the present embodiment.

In Figure 9, in response to the output of the error-containing code detection signal 22, the error detector 7 suspends an error detecting process, and the DMA control unit 2 suspends a data transfer from the buffer memory 4 to the syndrome calculator 5. The error corrector 6 outputs an one-code word error correction completion signal 23 when it completes error correction for one code word.

Figure 10 shows the procedure of horizontal error correction in one sector of the error correction device of the present embodiment.

The behavior of the error correction device will be described as follows with reference to Figure 10.

Step (d-1): the same process as at step (c-1) of Embodiment 2 is performed.

Step (d-2): the same process as at step (c-2) of Embodiment 2 is performed.

Step (d-3): the same process as at step (a-3) of Embodiment 1 is performed.

Step (d-4): the syndrome calculator 5 performs error-containing code detection for every transferred code word, and outputs the syndrome 16 to the error corrector 6. When an error-containing code word is detected, the syndrome calculator 5 outputs the error-containing code detection signal 22 to the error detector 7 and to the DMA control unit 2. On the other hand, the error detector 7 also executes error detection for each code word. Only when the error-containing code detection signal 22 has not been outputted, the mid-term results of error detection for each code word are stored in the mid-term result register 8. When the detection of error-containing code has been informed by the error-containing code detection signal 22, the error detector 7 suspends an error detecting process. At the same time, the syndrome calculator 5 informs the DMA control unit 2 of the detection of an error-containing code. The DMA control unit 2 suspends an output of the DMA request 23 to the bus control unit 3. The bus control unit 3 suspends a data transfer from the buffer memory 4 to the syndrome calculator 5.

Step (d-5): the same process as at step (a-5) in the prior art is performed.

Step (d-6): the same process as at step (b-6) in the first embodiment is performed.

Step (d-7): the same process as at step (a-7) in the prior art is performed.

Step (d-8): after putting the data bus 11 in commission, the bus control unit 3 reads the error-corrected data from the error corrector 6 and overwrites the data in the buffer memory 4. When error correction for one